| 1 | 2. (Once afficilited) A friction of fabricating a fiash friction y device as recited in claim 1, |
|----|---|
| 2 | wherein said step of forming a common source region on said substrate includes the steps of |
| 3 | patterning a photoresist disposed over said substrate to substantially define said |
| 4 | predefined area at which the common source region is to be formed; |
| 5 | implanting ions into said substrate to form said common source region using said |
| 6 | patterned photoresist as an implant mask; and |
| ,7 | removing said patterned photoresist. |
| | |
| 1 | 3. (Once amended) A method of fabricating a flash memory device as recited in claim 2, |
| 2 | wherein said ions implanted to form said common source region include arsenic ions. |
| | |
| ĺ | 4. (Once amended) A method of fabricating a flash memory device as recited in claim 1, |
| 2 | wherein said step of forming a common source region includes the steps of |
| 3 | forming a sacrificial oxide layer over said top surface of said substrate; |
| 4 | patterning a photoresist disposed over said substrate to substantially define said |
| 5 | predefined area at which the common source region is to be formed; |
| 6 | implanting ions into said substrate to form said common source region using said |
| 7 | patterned photoresist as an implant mask; and |
| 8 | removing said patterned photoresist and said sacrificial oxide layer. |
| | |
| 1 | 5. (Once amended) A method of fabricating a flash memory device as recited in claim 1, |
| 2 | wherein said step of implanting ions includes the steps of |
| 3 | forming a tunneling exide layer over each said top surface area of said substrate; |
| 4 | depositing a first polysilicon layer over said tunneling oxide layer; |
| 5 | depositing a nitride masking layer over said first polysilicon layer; |
| 6 | patterning and etching said nitride masking layer to expose first and second portions of |
| 7 | said first polysilicon layer, said exposed first and second portions substantially defining first and |
| 8 | second floating gate regions; and |
| 9 | implanting ions into said first and second floating gate regions to adjust said threshold |
| 10 | voltage; and |
| 11 | wherein the forming of said pair of floating gates includes the steps of |

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| 12 | forming a floating gate oxide layer over said first and second exposed portions of said |
|----|--|
| 13 | first polysilicon layer; |
| 14 | removing said nitride masking layer; |
| 15 | etching said first polysilicon layer and said tunneling oxide layer using said floating gate |
| 16 | oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling |
| 17 | oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said |
| 18 | substrate, said remaining portions of said first polysilicon layer forming first and second floating |
| 19 | gates associated with each said cell, said floating gates having side walls and a portion which |
| 20 | overlies a portion of said common source region thereby providing a high coupling ratio for the |
| 21 | associated cell. |
| BI | |
| 1 | 6. (Once amended) A method of fabricating a flash memory device as recited in claim 5, |
| 2 | wherein said step of forming said select gates includes the steps of |
| 3 | forming an insulating layer over the exposed portion of said substrate and the floating |
| 4 | gate oxide layer covering said floating gates; |
| 5 | forming a second polysilicon layer over said insulating layer; |
| 6 | forming a conductive layer over said second polysilicon layer; and |
| 7 | removing portions of said conductive layer, said second polysilicon layer, and said |
| 8 | insulating layer to form said select gates. |
| | |
| 1 | 7. (Once amended) A method of fabricating a flash memory device as recited in claim 6, |
| 2 | wherein said step of forming an insulating layer over said exposed portion of said substrate and |
| 3 | said floating gate oxide layer covering said floating gates includes the steps of |
| 4 | forming a first gate oxide layer over said exposed portion of said substrate, over said |
| 5 | floating gate oxide layer, and over said floating gates; |
| 6 | forming a nitride layer over said first oxide layer; |
| 7 | performing an etching process to remove a portion of said nitride layer and leaving |
| 8 | nitride spacers adjacent said side walls of each of said floating gates; and |
| 9 | forming a second gate oxide layer over said first oxide layer, over said nitride spacers and |
| 10 | over said floating gate oxide layer. |

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8. (Not amended) A method of fabricating a flash memory device as recited in claim 6, wherein 1 2 said conductive layer includes tungsten. 9. (Not amended) A method of fabricating a flash memory device as recited in claim 1, wherein 1 2 said ions includes Boron ions. 10. (Once amended) A method of fabricating a flash memory device as recited in claim 6, 1 wherein said step of forming drain regions associated with each cell includes the steps of 2 patterning and etching said conductive layer and portions of said substrate to substantially define the boundaries of drain areas of said substrate; and implanting ions into said drain areas to form said drain regions. 11. (Once amended) A method of fabricating a flash memory device as recited in claim 4, 1 wherein said step of implanting said ions into said substrate to form said common source region 2 3 includes: implanting arsenic ions to provide a dopant density in the range of 1 x 10¹⁴/cm2 to 5 x 4 10¹⁴/cm² and at an energy range of 80 to 150 KeV. 5 12. (Once amended) A method of fabricating a flash memory device as recited in claim 5, 1 wherein said step of depositing a first/polysilicon layer over said tunneling oxide layer includes: 2 3 depositing polysilicon upon said tunneling at a temperature of approximately 620 degrees 4 C in order to form said first polysilicon layer having a thickness in the range of 500 to 2500 5 angstroms. 13. (Not amended) A method of fabricating a flash memory device as recited in claim 12, 1 wherein said first polysilicon layer includes SiH4. 2 14. (Once amended) A/method of fabricating a flash memory device having a high coupling 1 ratio, comprising the steps of 2

forming a/sacrificial oxide layer over said top surface of said substrate;

providing a silicon substrate having a top surface;

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| 5 | patterning a photoresist layer disposed over said sacrificial oxade layer to substantially |
|----------|---|
| 6 | define a source region of the substrate; |
| 7 | implanting first ions into said substrate to form a common source region of said substrate |
| 8 | using the patterned photoresist layer as an implant mask; |
| 9 | removing said patterned photoresist layer and said sacrificial oxide layer to expose said |
| 10 | top surface of said substrate; |
| 11 | forming a tunneling oxide layer over the exposed top surface of said substrate; |
| 12 | depositing a first polysilicon layer over said tunneling oxide layer; |
| 13 | depositing a nitride masking layer over said first polysilicon layer; |
| 13 14 | patterning and etching said nitride masking layer to expose at least one first portion and |
| 15 | at least one second portion of said first polysilicon layer, said first and second exposed portions |
| 16 | substantially defining first and second floating gate regions; |
| 17 | implanting second ions into portions of said substrate defined by said first and second |
| 18 | floating gate regions and including opposite extremities of said common source region, in order |
| 19 | to adjust the threshold voltage of the flash memory device; |
| 20 | forming a floating gate oxide layer over said first and second exposed portions of said |
| 21 | first polysilicon layer; |
| 22 | removing said nitride masking layer; |
| 23 | etching said first polysilicon layer and said tunneling oxide layer using said floating gate |
| 24 | oxide layer as a mask leaving remaining portions of said first polysilicon layer and said tunneling |
| 25 | oxide layer disposed beneath said floating gate oxide layer, and exposing a portion of said |
| 26 | substrate, each said remaining portion of said first polysilicon layer forming a floating gate |
| 27 | having side walls, having a portion which overlies a portion of said common source region there |
| 28 | by providing a high coupling ratio for an associated cell; |
| 29 | forming a first gate oxide layer over said exposed portion of said substrate, over said |
| 30 | floating gate oxide layer, and over said floating gates; |
| 31 | forming a nitride layer over said first oxide layer; |
| 32 | performing an etching process to remove a portion of said nitride layer and leaving |
| 33 | nitride spacers adjacent said side walls of each of said floating gates; |
| 34 | forming a second gate oxide layer over said first oxide layer, over said nitride spacers and |
| 35 | over said floating gate oxide layer |

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| 36 | forming a second polysilicon layer over said second gate oxide layer; |
|-------------|--|
| 37 | forming a conductive layer over said second polysilicon layer; |
| 38 | removing portions of said conductive layer, said second polysilicon layer, said second |
| 39 | gate oxide layer, said nitride spacers and said first gate oxide layer to form a plurality of select |
| 4 0 | gates each having a portion overlying a portion of an associated one of said floating gates; and |
| 19 1 | patterning and etching said conductive layer to expose portions of said substrate to |
| 42 | substantially define the boundaries of at least one drain area of said substrate; and |
| 43 | implanting third ions into said drain area of said substrate to form at least one drain |
| 44 | region. |
| | |
| 1 | Cancel claim 15 without prejudice. |
| | |
| 1 | 16. (Once amended) A method of fabricating a flash memory device as recited in claim 14, |
| 2 | wherein said first fions include N-type ions and said additional ions include P-type ions, whereby |
| 3 | threshold voltage of the flash memory device is adjusted. |
| | |